UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,055	07/25/2003	Ryoji Suzuki	9792909-5648	2206

26263 7590 05/02/2007

SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,055	SUZUKI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 2/9/2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of prior Patent No. 6,677,993 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Drawings

2. The drawings filed on 2/9/2007 (Fig. 15) to include PRIOR ART legend is accepted.

Response to Arguments

3. Applicant's arguments filed 2/9/2007 have been fully considered but they are not persuasive.

The Applicant asserts, "The gate and drain electrodes of the reset transistor 3 are connected to a reset line 6, which is connected to the vertical scanning circuit 21 (col. 4, lines 64-67). The storage capacitors 11, 12 are connected to a horizontal signal line 20 through horizontal gate switch transistors 13, 14, which are sequentially scanned by a horizontal scanning circuit 22 (col. 4, lines 16-21). Akimoto et al. does not disclose or suggest the use of a horizontal scanning circuit serving as the reset element, said horizontal scanning circuit generating the reset pulse, as recited by amended claim 27. Rather, in Akimoto et al., the horizontal scanning circuit 22 affects the horizontal gate switch transistors, which operate the storage capacitors."

In response, the Examiner respectfully disagrees with the Applicant's assessment of the prior art. It is clear that the Applicant relies on Fig. 4 of Akimoto for the arguments. However, as clearly stated in the previous office action, the rejection is relied on the prior art **Fig. 3**, **not** **Fig. 4**. The Examiner submits that Akimoto still meets all limitations of amended claim 27. It should be noted that the Applicant appears to intend to include both the reset transistors 15, 16 and the horizontal scanning circuit 24 as said reset element (please see amended claim 27 which broadens the reset element to cover not only the reset transistors but also the horizontal scanning circuit illustrated by Fig. 1). Accordingly, the claimed "reset element" reads on the reset transistor 3 on line 52 and the horizontal scanning circuit 22 of Akimoto, wherein the horizontal scanning circuit 22 generates reset pulse to send to the gate of the reset transistor 3 via line 52 as shown in Fig. 3 and col. 2, line 54 – col. 3, line 24.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Akimoto et al. (US 4,942,474).

Regarding claim 27, Akimoto discloses a solid-state image sensor (**Fig. 3**, col. 2, line 54 – col. 3, line 24) comprising:

unit pixels each having a photoelectric conversion element (photodiode 1; Fig. 3) for converting incident light into an electric signal charge (col. 2, lines 56-60);

an amplifying element (pixel amplifier 4; Fig. 3) for amplifying said electric signal charge of said photoelectric conversion element into electric signal (col. 2, lines 60-68);

a reset element (reset transistor 3 in combination with reset line 52 and horizontal scanning circuit 22; Fig. 3) for resetting said photoelectric conversion element in response to a reset pulse (see col. 3, lines 2-10 and note that the reset transistor 3 is operated only in response to a reset pulse from the horizontal scanning circuit to the gate of reset transistor 3 via reset line 52);

a select switch (read-out switch 47; Fig. 3) for selectively outputting the electric signal from said amplifying element to a signal line (48) as a pixel signal (see col. 2, line 67 – col. 3, line 1);

a vertical scanning circuit (vertical scanning circuit 21; Fig. 3) for controlling said amplifying element (see col. 2, line 54 – col. 3, line 24, wherein the input and output of the pixel amplifier 4 are controlled by the vertical scanning circuit 21 through transistors 2 and 47 by signal lines 5, 45 and a signal line connected at the gate of transistor 47. Note in Fig. 3 that the pixel amplifier 4 is controlled to output an amplified signal when *at least* the output of the pixel amplifier 4 is turned ON by the vertical scanning circuit via signal line 45 and the gate of transistor 47 (ON state) so that the signal charge is properly and timely amplified and read out);

a horizontal scanning circuit (horizontal scanning circuit 22) serving as said reset element, said horizontal scanning circuit generating said reset pulse (see Fig. 3; col. 2, line 54 – col. 3, line 24, see Examiner's note for the reset element above).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner

DAVID OMETZ
SUPERVISORY PATENT EXAMINER